DNAe

LIVE DIAGNOSTICS

IC Layout Engineer

Job Reference:	ICEng/19	Location London, UK
Posted:	April 2019	Weekly Hours 40.0

The Role

At DNA Electronics Ltd, we are integrating cutting-edge semiconductor technologies with novel biochemical techniques to develop products for DNA analysis and molecular diagnostics. Our single-use sensor chip is being applied to detection and classification of bacteria in human blood.

The sensor chip is designed and developed at DNAe with all the necessary interaction with third party integrated chip manufacturing industries managed from within our team. This includes wafer fab, test and IC packaging.

You will be a key contributor to the design of the mixed-signal integrated circuits, responsible for the layout of individual circuit blocks as well as entire ICs, through to delivery of GDSII data to the fab.

Responsibilities – General

- Work with a multi-disciplinary team of design engineers on innovative custom cell layout in advanced process technologies.
- Work on full custom layout and verification of complex custom-designed cells.
- Responsibile for the chip floor planning, pin placement and die area management, custom cell and periphery layout, pad ring layout and ESD insertion, full-chip physical verification, tape out, and mask data verification.
- Setup or help to setup and manage the layout database.
- Work in very close collaboration with the IC design team, software development engineers, hardware development engineers, mechanical engineers, and scientists.
- Collaboration with external development and manufacturing partners in the UK and abroad.
- Manage the entire EDA flow with responsibility for keeping Cadence tools up-to-date and installing and maintaining foundry PDK's.
- Responsible for the team's tape-outs and liaison with the foundries as necessary.

Qualifications and experience

Required

- Excellent academic background in a relevant discipline.
- Experience in Analog /Mixed Signal full custom IC layout with a proven track record of full custom layouts in advanced CMOS technologies.
- Good understanding of layout design techniques in submicron CMOS processes.
- Solid understanding of physical, electrical, and DFM rules for CMOS processes. Experience of layout and schematic verification, and other physical and electrical design rules.
- Layout for low noise, low signal contamination.
- The ability to read and understand complex designs.
- Good understanding of isolation issues and ability to create effective shielding / isolation structures.
- Fully competent in the use of Cadence design tools (e.g. Virtuoso Layout editors and Assura or PVS DRC/LVS/RCX etc.).

Desirable

- Understanding of ESD and latch-up.
- A background in medical device development and understanding of legislative requirements (i.e., ISO13485).
- Performs well in a cross-functional cross-cultural team environment.
- Understands specific roles within the team and maintains both personal focus and group vision.
- Results oriented, flexible, drives subsystem and top-level layout tradeoffs required to meet deadlines.

Location

This role will be based in DNA Electronics headquarters, in West London at White City, W12 7SB.

Apply

If you meet the above criteria and would relish playing a key role in developing a revolutionary technology, we would be delighted to hear from you.

We offer a competitive compensation package to successful candidates.

Please email your CV, making a note of your salary expectations and availability in the email to: careers@dnae.com quoting the **job title and your name** in the subject line.

For more information about DNAe, please visit our website www.dnae.com